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Transmitted herewith for filing is the patent application of

Inventor(s): **Sitaram Yadavalli and Sandip Kundu**

For : **METHOD AND APPARATUS FOR MODELING AND CIRCUITS WITH ASYNCHRONOUS BEHAVIOR**

1. Enclosed are:

   a) 1 cover sheet, 9 sheets of specification, 3 sheets of claims, and 1 sheet of abstract;

   b) 7 sheets of drawings;

   c) Declaration and Power of Attorney (signed);

   d) Assignment

   e) Express Mail Certificate; and

   f) Return Receipt Postcard.

2. The filing fee has been calculated as shown below:

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INDEPENDENT CLAIMS	3 - 3=	0	78 00	00
MULTIPLE DEPENDENT CLAIM PRESENT			260 00	0
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Dated: 3-20-00

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PATENT APPLICATION

METHOD AND APPARATUS FOR MODELING AND CIRCUITS WITH ASYNCHRONOUS BEHAVIOR

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METHOD AND APPARATUS FOR MODELING CIRCUITS WITH ASYNCHRONOUS BEHAVIOR

by Inventors

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Background of the Invention

Field of the Invention

The present invention relates generally to modeling a logic gate level circuit. More particularly, the present invention relates to modeling the netlist modeling and a method of using sequential automatic test pattern generation for an asynchronous circuit to allow accurate testing.

Background of the Invention

Digital circuits typically undergo extensive operability testing. The testing is required because the presence of even one defective gate or transistor can ruin the reliability or even the functionality of a semiconductor chip. As chip speeds increase, circuits become more and more complex, therefore, it is often not practical and sometimes impossible to apply all possible tests to a chip.

Automatic test pattern generation (ATPG) is a computer implemented tool that is used to analyze complex integrated circuits such as combinational and synchronous sequential circuits. After a logic gate level description of the circuit (sometimes referred to as a netlist) is input to the computer, the ATPG then generates test patterns that are applied physically to the actual circuit by production testers. The test patterns are designed to reliably detect defects in the chip while applying the minimum number of tests. A good set of test patterns will be able to cover at least 90% of the chip.

Figure 1 is a logic gate level diagram of a digital circuit 1 with a feedback loop and a logic gate level netlist model 2 representing digital circuit 1. Digital circuit 1 includes an AND gate 4 having a number of inputs. One input of an OR gate 6 is coupled to an output of AND gate 4 by a first conductive path 8. An output of OR gate 6 is

coupled to one input of an AND gate 10 by a second conductive path 12, which is of greater length than first conductive path 8. An output of AND gate 10 is coupled to an input of OR gate 6.

Each equation in netlist model 2 represents a relationship between each gate in digital circuit 1. For example, C = A OR B represents the operation of OR gate 6. Netlist model 2 may be used by ATPG to simulate digital circuit 1, however it does not provide ATPG with any information regarding delays that may exist in digital circuit 1. Delays in circuits may be caused by varying factors including die and chip architecture constraints, the operational speed of each gate, the lengths of conductive paths between circuit elements, and the specific routing directions and positions of each element.

For example, in digital circuit 1, if second conductive path 12 is of much greater length than first conductive path 8, then a delay may be caused in the feedback loop. If the output of AND gate 10 is delayed, then the value of A may not have been updated when a new value for B arrives at OR gate 6. In another example, it is assumed that second conductive path 12 is much shorter than first conductive path 8 and AND gate 10 has a shorter delay than AND gate 4. In such a scenario, the output of AND gate 4 may be delayed so much that OR gate 6 operates on a new value of AND gate 10 and an old value of AND gate 4. This is known as a min-delay problem. Because there is a race between values of A and B to be input into OR gate 22, a race resolution mechanism must be used to correctly analyze and describe the operation of digital circuit 1.

However, in purely cycle based simulators or synchronous sequential ATPG systems, a mechanism for timing based race resolution is not available. ATPG systems do not have a concept of time beyond clock cycle pulses, therefore it is unable to resolve races between combination elements. Instead, ATPG tools rely on specific assumptions to perform race resolution between clock and data signals on latches or for delays in a combinational feedback loop. Because these assumptions are hard-coded in the software, the ATPG race resolution mechanism cannot be altered or redefined by the user. Therefore, using a test pattern generated by ATPG to test circuits with asynchronous behavior (including circuits that have time-borrowing or wave pipelining characteristics) will result in errors.

For example, if ATPG were used to generate test patterns for digital circuit 1, errors in testing would occur because there is no race resolution mechanism for OR gate 22. Not only would ATPG assume that one signal is arriving right after the other signal, it would also assume that the order in which signals arrive at OR gate 22 is arbitrary. Therefore, a test pattern generated by ATPG for digital circuit 1 would lead to errors in testing. In view of the foregoing, it is desirable to have a method and apparatus for modeling delays within a netlist or other circuit model to allow ATPG to generate a test pattern that is able to perform race resolution on circuits that exhibit asynchronous behavior either individually or collectively with other circuit elements.

Summary of the Invention

In one embodiment of the present invention, a netlist model of a physical circuit is provided. The netlist model includes a virtual delay element, wherein the virtual delay element is coupled to an asynchronous circuit element.

Brief Description of the Drawings

The present invention will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements.

Figure 1 is a logic gate level diagram of a digital circuit with a feedback loop and a logic gate level netlist model representing the digital circuit.

Figure 2 is a block diagram of a computer system for generating a model digital circuit in accordance with one embodiment of the present invention.

Figure 3A is a diagram of a model digital circuit for ATPG in accordance with one embodiment of the present invention.

Figure 3B illustrates a logic gate level netlist model and a Verilog netlist representing model digital circuit illustrated in Figure 2.

Figure 4 is a diagram of a model sequential circuit with race resolution in accordance with one embodiment of the present invention.

Figure 5 is a diagram of a model bypass circuit having delay sensitive combinational feedback loops with race resolution in accordance with one embodiment of the present invention.

Figure 6 is a flowchart of a method for generating a model for a circuit in accordance with one embodiment of the present invention.

Detailed Description

A method and apparatus for netlist modeling for ATPG in circuits with asynchronous behavior. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be understood, however, to one skilled in the art, that the present invention may be practiced without some or all of these specific details. In other instances, well known process operations have not been described in detail in order not to unnecessarily obscure the present invention.

Figure 2 is a block diagram of a computer system 14 for generating a model digital circuit in accordance with one embodiment of the present invention. Computer system 14 includes a network or bus 16, which is coupled to a central processing unit (CPU) 18 and a memory unit 20. Network 16 is also coupled to a storage medium 21 and a number of input/output (I/O) devices 22.

Data is transferred along network 16 to and from each of the other components in computer system 14. Data representing a physical circuit to be tested is input by I/O devices 22 to memory 20. A program for generating a netlist model for the circuit is input to memory 20 from storage medium 16. CPU 18 runs the program and outputs the netlist model to I/O devices 22, so that the netlist may be used in ATPG. The program for generating the netlist model is described below in greater detail.

Figure 3A is a diagram of a model digital circuit 1' for ATPG in accordance with one embodiment of the present invention. In addition to the elements present in the actual physical digital circuit 1, modeled digital circuit 1' further includes a virtual delay element 24 having an input coupled to a virtual clock vclk1 and a virtual delay element 26 having an input coupled to a virtual clock vclk2. Virtual delay element 24 is also coupled to the output of AND gate 10 and to the input of OR gate 6 along first conductive path 8. Virtual delay element 26 is coupled to the input of AND gate 10 and the output of OR gate 6 along second conductive path 12.

Through virtual delay elements 24 and 26, a user may impose a specific race resolution through virtual clocks that have timing characteristics that are controlled as

virtual primary inputs. For example, if in digital circuit 1, data traveling on second conductive path 12 takes a long time relative to data traveling on first conductive path 8, then a rising edge of vclk2 may be set at a later time than a rising edge of vclk1 to resolve the race. It is in this manner that a user may impose an order as to which set of data arrives at the inputs of OR gate 6 first. The sequential ATPG tool can then obtain the appropriate test vectors while satisfying the virtual clock constraints provided by the user. By using model digital circuit 1' as a model for a netlist, ATPG may successfully generate valid test patterns for digital circuit 1.

Figure 3B illustrates a logic gate level netlist model 27 and a Verilog netlist 28 representing model digital circuit 1' illustrated in Figure 2. Netlist model 2 of digital circuit 1 from Figure 1 is incorporated into netlist model 27. Netlist model 27 also includes virtual delay elements 24 and 26, which are described as flip-flops that latch the values at inputs in_{24} and in_{26} to outputs out_{24} and out_{26} when vclk1 and vclk2 are high. In Verilog netlist 28, vclk1 and vclk2 are designated as a type of wire and implicitly used as control points for an ATPG tool. This is equivalent to declaring them as and using them as primary inputs.

Figure 4 is a diagram of a model sequential circuit 29 with race resolution in accordance with one embodiment of the present invention. The "real" elements of model sequential circuit 29 include a flip-flop 30 with a clock clk input and a data1 input. The output of flip-flop 30 is coupled to the input of an AND gate 32. Another input of AND gate 32 is coupled to the clk. The output of AND gate 32 is coupled to the clock input of a flip-flop 34, which has a data2 input. Model sequential circuit 29 also includes a virtual delay element 36 coupled between the clock source and the clock input of flip-flop 30. Virtual delay element 36 has a clock input, which is coupled to a virtual clock vclk.

If an updated value of data1 is different than the old value of data1, then the output of flip-flop 30 will be different depending on whether the updated data1 signal or the rising edge of the clk pulse wins the race to the input of flip-flop 30. In the following example, the clock-to-output delay of flip-flop 30 is less than the delay of AND gate 32 and the old value of data1 is "1" and an updated value of data1 is "0". If the rising edge of the clk pulse wins the race, then flip-flop 30 will continue to latch the old value "1",

which propagates to AND gate 32. AND gate 32 will then evaluate to a "1" and allow data2 to be latched in flip-flop 34. If the "1" value on the clock input of flip-flop 30 arrives after the new "0" value on data1, then flip-flop 30 will latch "0" to AND gate 32, which outputs a "0" disabling flip-flop 34.

Because ATPG assumes an arbitrary winner of the race, it will not generate a successful test pattern that reflects the actual operation of sequential circuit 29. Therefore, the addition of virtual delay element 36 in a netlist model is used to resolve the race between the data and clock inputs of flip-flop 30 for ATPG. Virtual delay element 36 may be used to delay the rising edge of clk from reaching flip-flop 30 until vclk is asserted to impose a specific race resolution. The relationship between vclk and the other components of model sequential circuit 29 may be specified by the user depending on the exact delay characteristics of the physical circuit. The actual vclk pulse may be asserted by the user or it may be generated by ATPG.

According to an embodiment of the present invention, race resolution at every sequential element can be individually controlled by the introduction of virtual delay elements controlled by corresponding virtual clocks in the appropriate path. Therefore, each sequential element can have its own race resolution mechanism. For example in sequential circuit 29, if control over the arrival time of data1 is required by ATPG, then a virtual delay element 38 may be added along the path of the data1 input to flip-flop 30.

Figure 5 is a diagram of a model bypass circuit 40 having delay sensitive combinational feedback loops with race resolution in accordance with one embodiment of the present invention. Model bypass circuit 40 includes a pair of registers 42 and 44, which output to a corresponding pair of multiplexers (MUX) 46 and 48. Multiplexers 46 and 48 have outputs that are coupled to a pair of virtual delay elements 50 and 52. Virtual delay elements 50 and 52 are enabled by virtual clocks vclk2 and vclk3 to output data to an arithmetic logic unit (ALU) 54. ALU 54 performs an arithmetic operation on the data and outputs the data to a register 56. The circuit includes a virtual delay element 58 enabled by vclk1. Virtual delay element 58 then completes a feedback loop by outputting data to multiplexer 48.

Model bypass circuit 40 is an example of an asynchronous circuit where time borrowing occurs and virtual delay elements 50, 52, and 58 are required to model a netlist for ATPG. If for example, ALU 54 is attempting to perform an adding operation such as: sum = A + B + C, then the operation may be broken up into two separate operations represented by: sum1 = A + B and sum2 = sum1 + C. The intermediate result (sum1) may be sent directly to multiplexer 48 without being stored by register 56. Therefore, one part of the feedback loop in model bypass circuit 40 will be borrowing time from another part to generate the end result. If virtual delay elements 50, 52, and 58 are not present in the netlist, then ATPG will not take time borrowing and min-delay in the bypass loop into account, and the test pattern generated will not function properly.

Figure 6 is a flowchart of a method 60 for generating a model for a circuit in accordance with one embodiment of the present invention. Method 60 begins at a block 62, in which a netlist model is generated for the circuit. The netlist model is a logic gate level description of the circuit that is used by ATPG to generate test patterns that are applied to the actual circuit to test for defects. In a block 62, a virtual delay element is provided to the netlist model. The virtual delay element is coupled to an asynchronous circuit element (or a combination of circuit elements that demonstrate asynchronous behavior) and provided along paths where race resolution is required. By controlling a virtual clock that enables the virtual delay element, either the user or ATPG may impose an order in which signals arrive at any component in the circuit.

An advantage of the present invention is that it allows for race resolution in an ATPG system for circuits that exhibit asynchronous behavior. The ATPG system will then be able to generate valid test patterns to test the circuits for defects. Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention. Furthermore, certain terminology has been used for the purposes of descriptive clarity, and not to limit the present invention. The embodiments and preferred features described above should be considered exemplary, with the invention being defined by the appended claims.

What is claimed is:

1. A netlist model of a physical circuit comprising:

a virtual delay element, wherein said virtual delay element is coupled to a circuit element in said physical circuit.

2. A netlist model of a physical circuit as recited in claim 1, wherein an input signal is supplied to the virtual delay element.

3. A netlist model of a physical circuit as recited in claim 2, wherein the input signal is supplied by a test pattern generator.

4. A netlist model of a physical circuit as recited in claim 2, wherein the input signal is supplied by a user.

5. A netlist model of a physical circuit as recited in claim 3, wherein the netlist model is used by a test pattern generator to generate a test pattern for the physical circuit.

6. A netlist model of a physical circuit as recited in claim 4, wherein the netlist model is used by a test pattern generator to generate a test pattern for the physical circuit.

7. A netlist model of a physical circuit as recited in claim 2, wherein the virtual delay element is one of a flip-flop or a latch.

8. A method for generating a model for a physical circuit comprising:

generating a netlist model for said physical circuit; and

providing a virtual delay element to said netlist model, wherein said virtual delay element is coupled to a physical circuit element.

9. A method for generating a model for a physical circuit as recited in claim 8, further comprising providing an input signal for said virtual delay element.

10. A method for generating a model for a physical circuit as recited in claim 9, wherein the input signal is supplied by a test pattern generation system.

11. A method for generating a model for a physical circuit as recited in claim 9, wherein the input signal is supplied by a user.

12. A method for generating a model for a physical circuit as recited in claim 10, wherein the netlist model is used by a test pattern generator to generate a test pattern for the physical circuit.

13. A method for generating a model for a physical circuit as recited in claim 11, wherein the netlist model is used by a test pattern generator to generate a test pattern for the physical circuit.

14. A method for generating a model for a physical circuit as recited in claim 9, wherein the virtual delay element is one of a flip-flop or a latch.

15. A set of instructions residing in a storage medium, said set of instructions capable of being executed by a processor to implement a method for generating a model for a physical circuit, the method comprising:

generating a netlist model for said physical circuit; and

providing a virtual delay element to said netlist model, wherein said virtual delay element is coupled to an asynchronous circuit element.

16. A set of instructions residing in a storage medium as recited in claim 15, wherein the method for generating a model for a physical circuit further comprises providing an input signal for said virtual delay element.

17. A set of instructions residing in a storage medium as recited in claim 16, wherein the input signal is supplied by a test pattern generation system.

18. A set of instructions residing in a storage medium as recited in claim 17, wherein the input signal is supplied by a user.

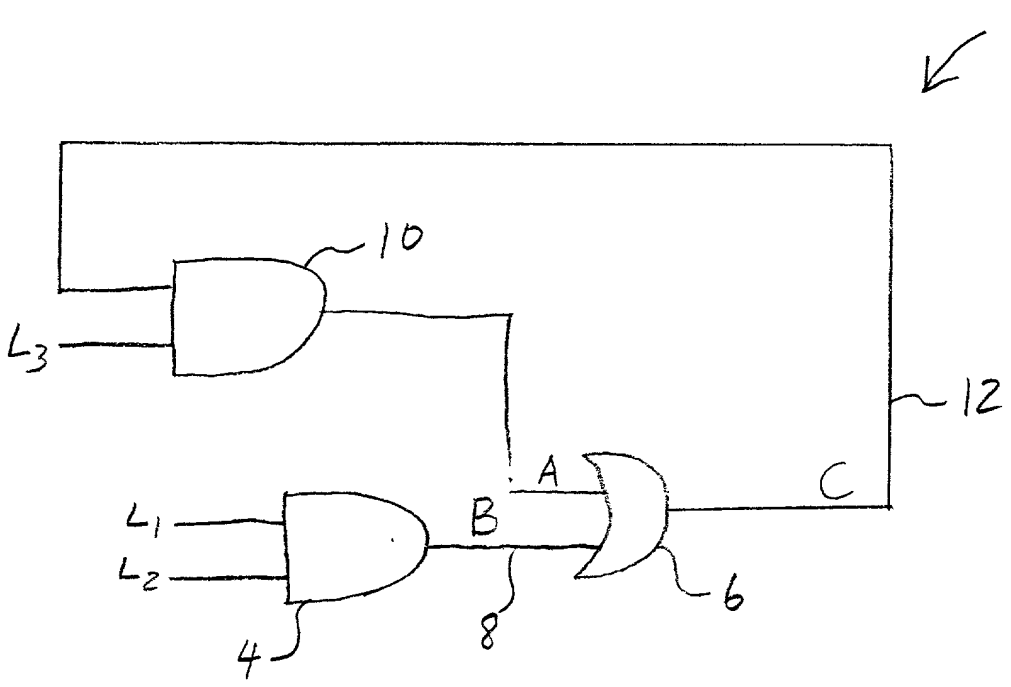
19. A set of instructions residing in a storage medium as recited in claim 17, wherein the netlist model is used by a test pattern generator to generate a test pattern for the physical circuit.

20. A set of instructions residing in a storage medium as recited in claim 18, wherein the netlist model is used by a test pattern generator to generate a test pattern for the physical circuit.

21. A set of instructions residing in a storage medium as recited in claim 16, wherein the virtual delay element is one of a flip-flop or a latch.

Abstract of the Disclosure

A netlist model of a physical circuit is provided. The netlist model includes a virtual delay element, wherein the virtual delay element is coupled to an asynchronous circuit element.



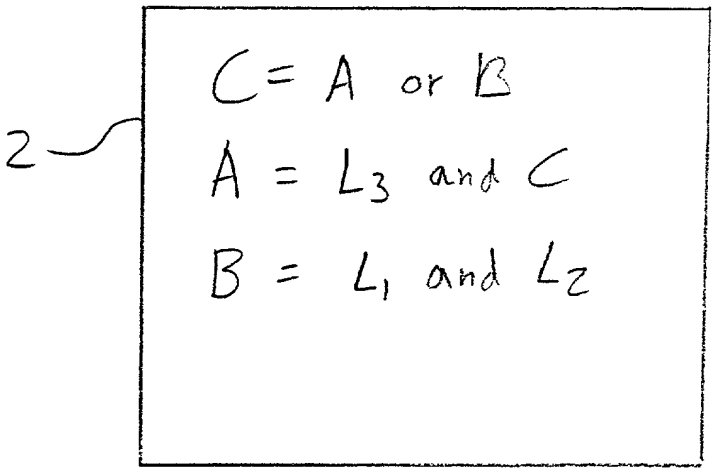


Fig. 1
(Prior Art)

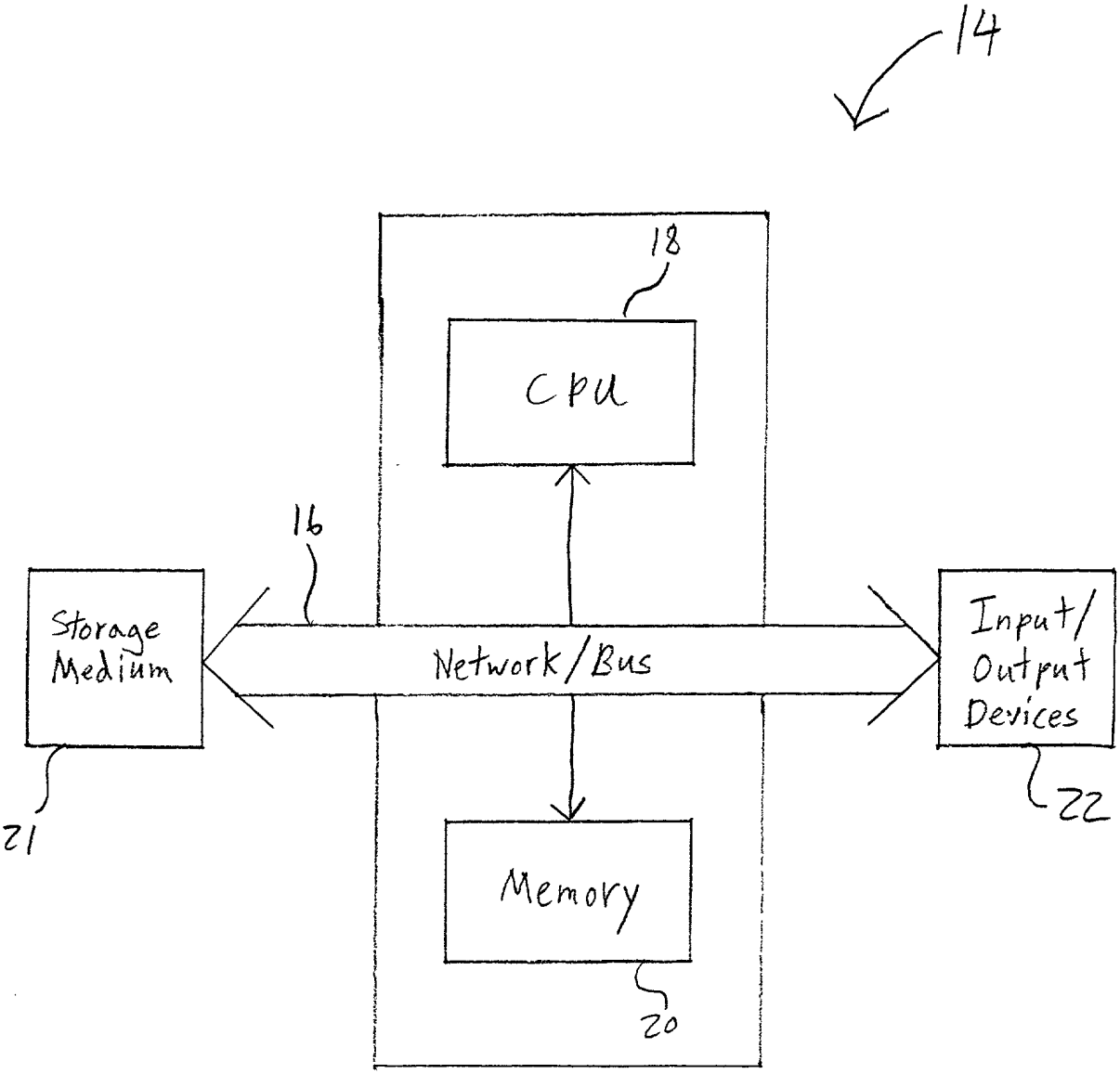

14
18
CPU
16
Storage Medium
Network/Bus
Input/ Output Devices
Memory
21
22
20

Fig. 2

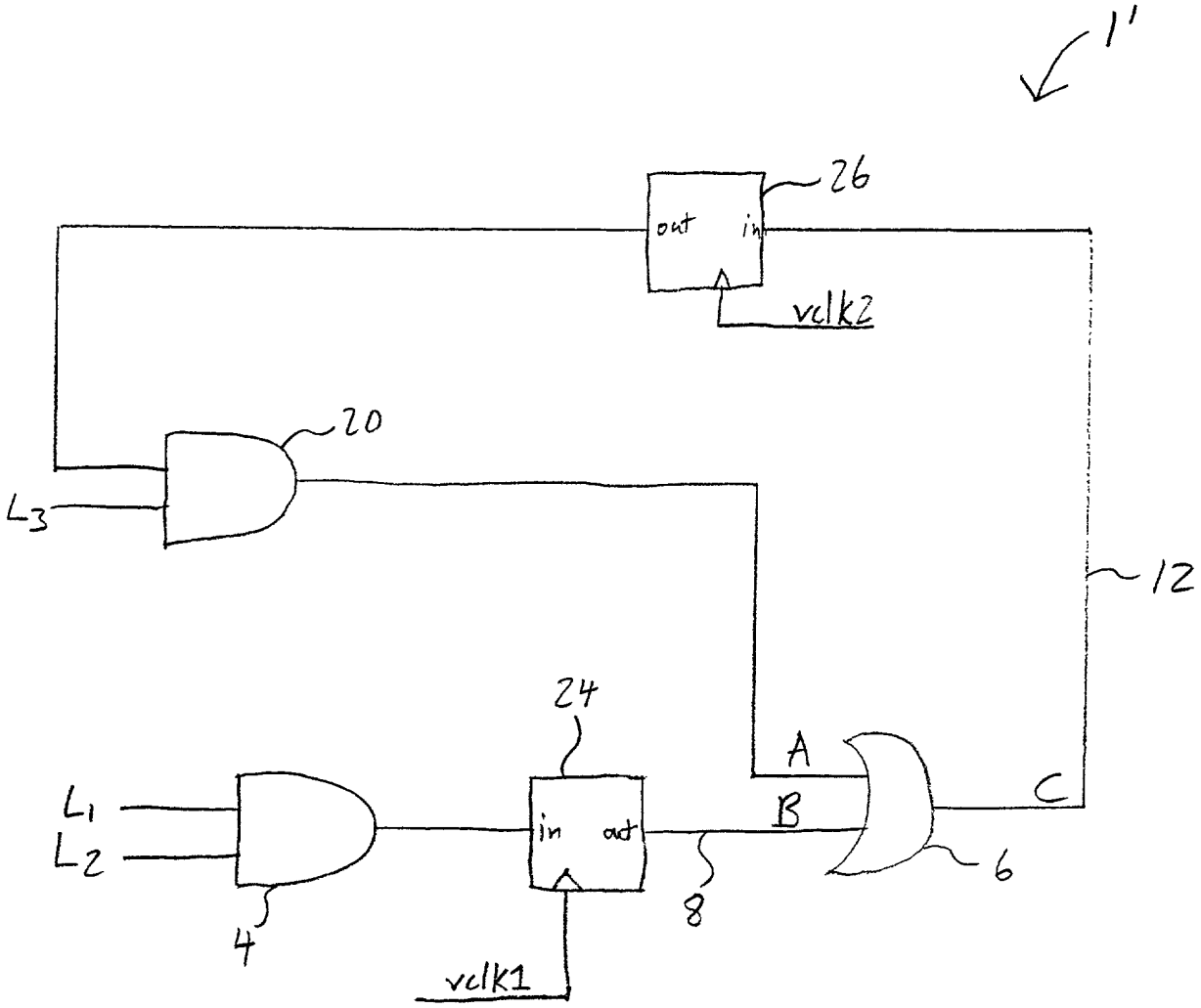


Fig. 3A

in_{24} = L_1 and L_2
out_{24} = if (vclk1 == HIGH) then in_{24}//change state
else out_{24}//retain state
B = out_{24}
C = A or B
in_{26} = C
out_{26} = if (vclk2 == high) then in_{26}//change state
else out_{26}//retain state
A = L_3 and out_{26}

~27

```
module fig1 ( L1, L2, L3, vclk1, vclk2, .. )
input L1, L2, L3, vclk1, vclk2;

        and     g14 ( in24, L1, L2 );
        vdelement g24 ( out24, vclk1, in24 );
        or      g16 ( in26, A, out24 );
        vdelement g26 ( out26, vclk2, in26 );
        and     g20 ( A, L3, out26 );

endmodule


primitive vdelement (out, vclk, in)
output out;
reg out;
input vclk, in;

table
// vclk  data   out     out_new
  1      1 :    ?       : 1 ;
  1      0 :    ?       : 0 ;
  0      ? :    ?       : - ; // - means 'no change', i.e. retain previous value
endtable
endprimitive
```

~28

Fig. 3B

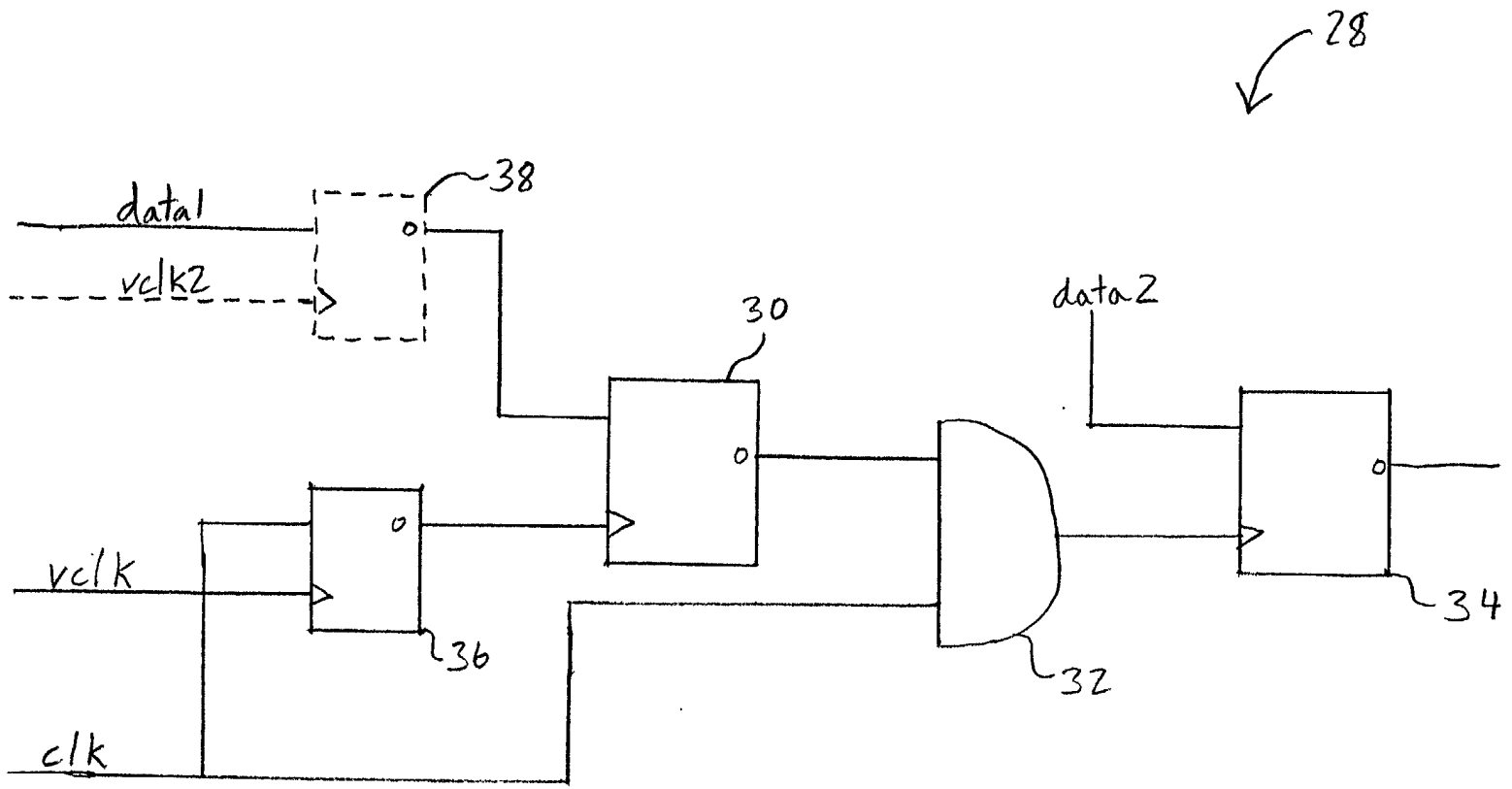


Fig. 4

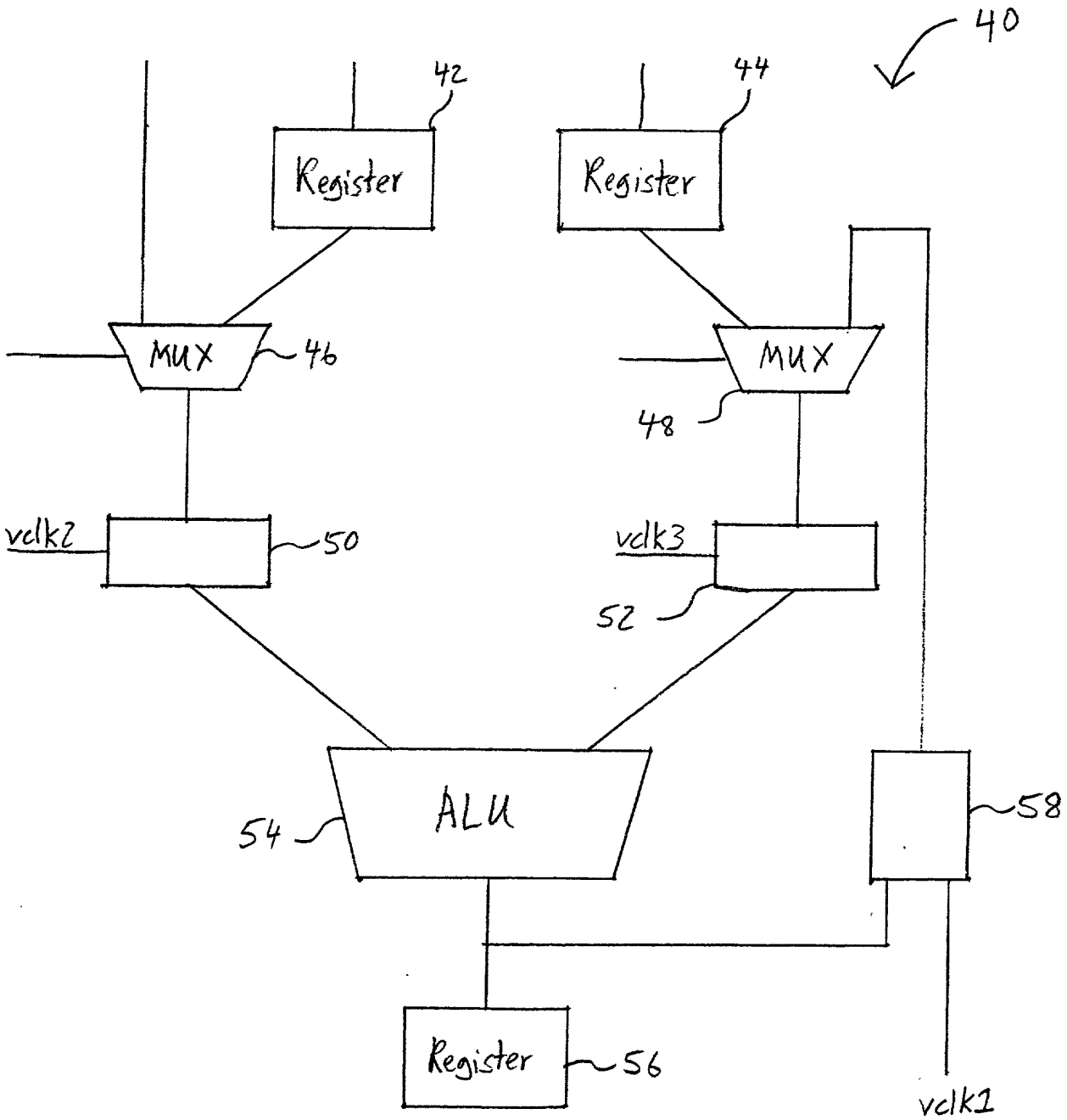

40
42
44
Register
Register
MUX
46
MUX
48
vclk2
50
vclk3
52
ALU
54
58
Register
56
vclk1

Fig. 5

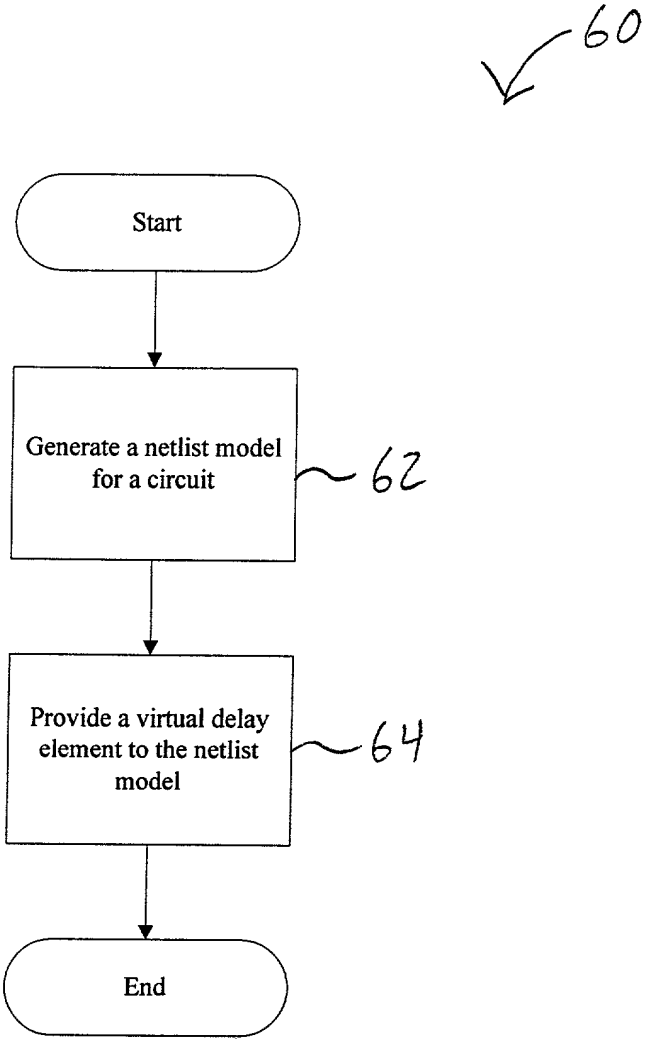

60
Start
Generate a netlist model for a circuit
62
Provide a virtual delay element to the netlist model
64
End

Figure 6

PATENT

Docket No. 2207/7896

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD AND APPARATUS FOR MODELING AND CIRCUITS WITH ASYNCHRONOUS BEHAVIOR

the specification of which is attached hereto unless the following is entered:

was filed on	as United States Application Number or PCT International Application Number	and was amended on (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR §1.56.

PRIOR FOREIGN APPLICATION(S)

I hereby claim foreign priority benefits under 35 USC §119(a-d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below any foreign application(s) for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed:

Application Number	Country	Filing Date (day/month/year)	Priority Not Claimed

PROVISIONAL APPLICATION(S)

I hereby claim the benefit under 35 USC §119(e) of any United States provisional application(s) listed below:

Application Number		Filing Date	

PRIOR UNITED STATES APPLICATION(S)

I hereby claim the benefit under 35 USC §120 of any United States application(s), or §365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 USC §112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR §1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

Application Number	Filing Date	Status (patented, pending, abandoned)

POWER OF ATTORNEY

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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PATENT
Docket No. 2207/7896

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION (Cont.)

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I hereby declare that all statements made herein of my own knowledge are true and all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code and that such willful statements may jeopardize the validity of the application or any patent issuing thereon.

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Signature Y. Sitaram		Date March 13, 2000	
Full name of second inventor	Last Name **KUNDU**	First Name **SANDIP**	Middle Name
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Signature Sandip Kundu BTWJF		Date 3/16/00	
Full name of third inventor	Last Name	First Name	Middle Name
Residence	City	State or Country	Country of Citizenship
Post Office Address	Street	City	State or Country & Zip Code
Signature		Date	
Full name of fourth inventor	Last Name	First Name	Middle Name
Residence	City	State or Country	Country of Citizenship
Post Office Address	Street	City	State or Country & Zip Code
Signature		Date	